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Test Technology of Automotive Grade Chip: Methods, Challenges and Applications

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Abstract: With the development of automobile electronization and intelligence, the reliability and performance of automobile grade chip are very important. This article provides an in-depth exploration of the current status, challenges, and applications of automotive specification chip testing technology. Firstly, the traditional testing methods, such as functional verification, performance evaluation, single chip testing, defect screening and electrical parameter verification, are summarized, and the advanced testing technologies, including energy-saving test optimization, multi-layer and vertical chip testing, embedded core component testing and intelligent and automatic means, are introduced. Secondly, it analyzes the technical challenges faced by the chip test of automotive regulation level, such as the increase of chip complexity, the stability in extreme environment and the safety requirements of automatic driving function; Cost challenges, such as the increase in test coverage and complexity; And standardization challenges, such as the update of international standard system and the particularity of RF chip testing. Finally, through the application of 3D stacked chips in the intelligent cockpit controller and the functional safety test case of MCU based on ISO26262, the practical application of the car-gauge chip test technology is demonstrated. The purpose of this paper is to provide reference for the development of chip testing technology for automotive specifications, and to promote the progress of related technologies, thus contributing to the safe and reliable development of the automobile industry.

Keywords: Automotive Grade Chip, Methods, Challenges, Applications.

1. Introduction

With the rapid development of automobile industry, the electronization and intelligentization of automobiles have become an irreversible trend. In modern cars, electronic control systems and intelligent driving assistance systems are becoming more and more popular, which makes the demand for high-performance and high-reliability electronic chips increase sharply. As the core component of automotive electronic system, the performance and reliability of automotive gauge chip are directly related to the safety and stability of automobile. Therefore, it is particularly important to carry out strict and effective testing on the car gauge chip. However, compared with consumer-grade chips, car-grade chips are facing more severe working environment and higher performance requirements. For example, the car gauge chip needs to work stably under extreme temperature, high humidity, strong vibration and other harsh conditions, and also needs to have extremely high reliability and long service life. These special requirements have brought great challenges to the test of automotive specification chip.

Although a variety of chip testing methods and technologies have been applied to the chip testing of automotive specifications, there are still some problems to be solved urgently. For example, how to improve the test coverage to ensure the reliability of the chip under various working conditions? How to reduce the test cost while ensuring the test quality? How to deal with the test problems brought by increasingly complex chip design and diversified application scenarios? These problems not only restrict the development of chip testing technology for automotive specifications, but also affect the progress of the whole automobile industry. The purpose of this paper is to deeply discuss the present situation, challenges and applications of the chip testing technology for automotive regulations. It is hoped that through the research of this paper, some useful references can be provided for the development of chip testing technology for automotive specifications, and the progress of related technologies can be promoted, thus contributing to the safe and reliable development of the automobile industry.

2. Test Method of Automotive Gauge Level Chip

2.1. Traditional Testing Method

(1) Functional verification and performance assessment

In the final test, the packaged chip is comprehensively tested, including open-short circuit test, DC parameter measurement and dynamic response analysis, so as to check the functional defects. At the same time, its stability under extreme conditions is evaluated, such as speed classification, noise suppression level and thermal stress tolerance [1].

(2) Single chip test

In-depth research is carried out for specific automotive electronic components, and potential problems are further explored by means of boundary scanning diagnosis, self-test and pressure loading test to ensure that they meet the strict requirements of automotive regulations.

(3) Defect screening and packaging integrity test

Using burning test, fault location and signal integrity test to find and repair the hidden dangers inside the chip; Through mechanical shock, vibration and temperature cycling tests, the reliability and transportation durability of the packaging structure are verified [2].

(4) Electrical parameter verification

The input and output voltage range, current consumption, working frequency and signal response are detected to ensure that the performance of the chip meets the design specifications under normal working conditions.

2.2. Advanced Testing Technology

(1) Energy saving test optimization

Using low-power automatic test mode generation to reduce circuit activity and lower power consumption; Adopting scanning path segmentation, adaptive signal control, or gate clock technology to achieve high-performance management testing scheme [3]; Introduce data compression methods to reduce the amount of testing data and energy consumption.

(2) Multilayer and vertical chip testing

For 3D stacked chips (using silicon via TSV technology), phased inspection is implemented: screening qualified grains before bonding, monitoring stacking process defects during bonding, verifying interlayer interconnection and overall function after bonding, and optimizing heat dissipation design to meet thermal management challenges [4]; Special attention is paid to TSV manufacturing defects (short circuit/open circuit caused by micropores and pinholes) and electrical performance degradation caused by wafer thinning.

(3) Embedded core component testing

Based on the IEEE Std 1500 standard, control and observation of IP cores within a System on Chip (SoC) are achieved through testing wrappers, access mechanisms, and Core Test Language (CTL). For example, using wrapper instruction registers to switch test modes, accelerating data register transfers, and monitoring internal states of core data registers [5].

(4) Intelligent and automatic means

Combined with digital twinning technology, the whole life cycle test database is established to support multi-physical field coupling simulation; Micro-and nano-scale measurement equipment is used to improve the detection accuracy of packaging defects to sub-micron level and enhance the cross-scale analysis ability [6].

2.3. Test Procedures and Standards

AEC-Q100 series standards must be passed, covering accelerated environmental stress test (group A), life cycle simulation test (group B) and manufacturing reliability test (group D), including high/low temperature cycling, wet-heat aging, electromagnetic compatibility and other experiments; Follow the quality management system IATF 16949 to ensure the controllability of the whole process from wafer manufacturing to packaging; Meet the functional safety standard ISO26262, strengthen fault self-diagnosis and redundant design; Early failure rate testing requires a large number of sample statistics, with an overall cycle of more than six months. If problems are found, they will be iterated again; Complete consistency verification of three batches of products before mass production, and generate AEC-Q test reports as the basis for admission [7]; Reserve performance margin to cope with wide temperature range fluctuations in the automotive environment (-40 ℃~+150 ℃); Integrating anti electromagnetic interference shielding structures and protection circuits to enhance stability in complex electronic environments.

3. Challenges Faced by The Chip Test of Automotive Specification Level

3.1. Technical Challenge

The chip test of automotive specification level faces multiple technical challenges. First of all, with the transformation of automobile industry to intelligence and electrification, the complexity of on-board semiconductor system is increasing, which puts forward higher requirements for the quality and reliability of chips. Especially in the application background of advanced process nodes, zero defect rate has become an unshakable quality goal, which poses unprecedented challenges to test design, fault model update and on-site self-inspection mechanism. Secondly, the car gauge chip needs to run stably in extreme environment, such as withstanding the temperature difference challenge of -40 to 125 degrees. In addition, with the transition from L2/L3 assisted driving to L4 or even L5 automatic driving, the functional complexity of the automotive-mounted system has doubled, and how to ensure the long-term stable operation of the control unit under extreme working conditions has become an unavoidable problem in the engineering field.

3.2. Cost Challenge

The cost challenge of automotive code level chip testing is mainly reflected in two aspects. On the one hand, in order to ensure the high reliability of the chip, the test coverage and the complexity of test methods are increasing, which leads to the increase of test time and the rising cost. On the other hand, with the increase of the number of chips and the variability and defect sensitivity brought by advanced technology, the quality threshold of a single chip has to be raised, which further increases the testing cost.

3.3. Standardization Challenge

First of all, the international automobile industry has formed a number of authoritative standard systems, such as AEC-Q100 series standards. These standards set up the entry threshold for car gauge chips from multiple dimensions, such as reliability testing of car gauge components, whole-process quality management, conceptual design, failure prevention and management process of scrap recycling life cycle [8]. However, with the development of technology and the change of market demand, these standards need to be constantly updated and improved to meet the new testing requirements. Secondly, the test of RF chips is not simply based on general standards, and its particularity is mainly reflected in the sensitivity of performance parameters and frequency dependence. This requires testing not only to confirm that the chip can work, but also to accurately quantify whether the parameter drift range meets the strict tolerance requirements of automotive regulations.

4. Application Case of Chip Testing Technology for Automotive Specification Level

4.1. Case 1: Test Application of 3D Stacked Chips in Intelligent Cockpit Controller

The intelligent cockpit system of a high-end automotive adopts a 3D stacked chip based on TSV technology, which integrates CPU, GPU and multiple storage units. In order to ensure its reliability in harsh environments such as alternating

high and low temperatures and vibration, a phased test strategy is adopted:

(1) Perform electrical parameter testing and defect screening on each wafer before bonding to select qualified grains;

(2) Monitoring during bonding involves real-time detection of thermal stress and connection defects during the stacking process through infrared thermal imaging and electrical signal monitoring;

(3) Perform overall functional verification, interlayer interconnection testing, and heat dissipation performance evaluation through post bonding testing.

The test results show that the performance of the chip is stable in the temperature range of -40℃ to 125℃, and the failure rate is less than 10 DPPM (Defective Parts Per Million), which meets the AEC-Q100 Grade 1 standard. As can be seen from Table 1, the test data of each stage show that the pass rate of electrical parameters before bonding is 99.2%, the pass rate of thermal stress monitoring during bonding is 98.5% and there is no abnormality in infrared imaging, and the pass rates of function verification and temperature cycle test after bonding are 99.8% and 99.6% respectively. All interfaces communicate normally without performance attenuation, and the overall yield and reliability meet the requirements of automotive specification application.

Table 1. Summary of test data of 3D stacked chips

Testing phase	Test item	Passing rate	Remarks
Before bonding	Electrical parameter test	99.2%	Voltage/current/frequency
Bonding	Thermal stress monitoring	98.5%	Infrared imaging is normal
After bonding	Functional verification	99.8%	All interfaces are communicating normally
After bonding	Temperature cycling test (-40~125℃)	99.6%	No performance attenuation

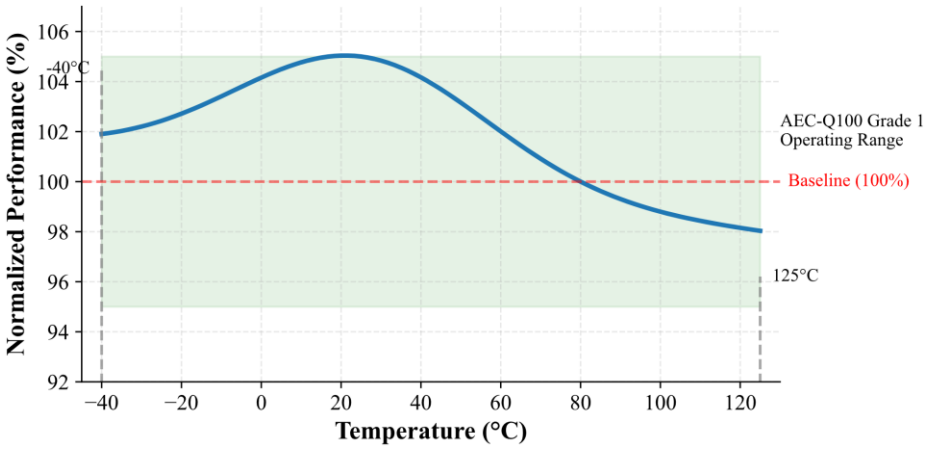

Figure 1. Effect curve of temperature on chip performance

The performance trend analysis in Figure 1 above shows that the car-gauge chip shows excellent stability in the full temperature range from -40℃ to 125℃, and the performance fluctuation is controlled between 95% and 105%, which fully meets the requirements of AEC-Q100 Grade 1 standard. Specifically, the performance of the chip in the low-temperature range (-40 ℃ to 0 ℃) is slightly higher than the benchmark (up to 104.5%), which helps to improve the startup capability in cold environments. The performance in the normal temperature range (20 ℃ to 40 ℃) remains stable around the 100% benchmark, while in the high-temperature range (>80 ℃), although it shows a slight downward trend with increasing temperature, it still maintains a performance level of 96.2% at an extreme high temperature of 125 ℃; The overall performance change amplitude is less than 5%, which not only verifies its reliability in extreme environments in automotive applications, but also reflects the engineering rationality of low-temperature performance gain and high-temperature moderate frequency reduction as safety mechanisms.

4.2. Case 2: Functional Safety Test of MCU Based on ISO 26262

A certain car company has adopted a microcontroller unit (MCU) that complies with ISO 26262 ASIL-D level in its electric power steering system (EPS). During the testing process, the focus was on implementing Fault Injection Testing (FIT) and redundancy design verification. Simulate various fault scenarios through the Hardware in the Loop (HIL) platform, such as power fluctuations, signal interruptions, memory errors, etc; Real time detection and isolation of faults using embedded self-test mechanism; Verify the system's fault response time and recovery capability.

Table 2 shows that the test results show that the MCU can respond correctly in 99.99% fault injection scenarios and enter a safe state, and the average fault detection time is less than 5ms, which fully meets the functional safety requirements.

Table 2. Statistics of MCU fault injection test results

Fault type	Injection times	Detection success rate	Average response time (ms)
Power supply voltage drop	200	100%	3.2
Signal wire short circuit	150	99.3%	4.1
Memory bit flip	300	98.7%	2.8
Clock signal failure	100	100%	5.0

The test results of MCU fault injection show that the

system has excellent detection ability and fast response performance in all kinds of fault scenarios. The detection success rate reached 100% in 200 power supply voltage drop tests, and the average response time was 3.2ms; The success rate of 150 signal line short circuit tests is 99.3%, and the response time is 4.1ms; The success rate of 300 memory bit flip tests is 98.7%, and the response time is only 2.8ms; The 100 clock signal failure tests also achieve 100% detection, and the response time is 5.0 ms. The overall test results verify the high reliability and real-time performance of the MCU in key safety indicators.

5. Conclusion

In this paper, the test technology of automotive code level chip is deeply discussed, including its methods, challenges and practical applications. The research results show that with the rapid transformation of the automobile industry to electronic and intelligent, the stability and high reliability of the car gauge chip in extreme environment have become the key requirements. Traditional testing methods, such as functional verification, single-chip testing and defect screening, are effective, but they have limitations in the face of complex design and harsh environment. Advanced testing technologies, such as energy-saving test optimization, multi-layer and vertical chip testing and embedded core component testing, have significantly improved the testing efficiency and accuracy. However, there are still many technical challenges in automotive code level chip testing, including increased complexity, extreme environmental adaptability requirements and strengthening of functional safety standards. In addition, the problems of testing cost and standardization also need to be solved urgently. Through application case analysis, such as the test of 3D stacked chips in intelligent cockpit controller and the functional safety test of MCU based on ISO 26262, the effectiveness and necessity of advanced testing technology are verified. In order to meet the growing challenges and ensure the safe and reliable operation of automotive electronic systems, the testing technology of automotive-level chips needs constant innovation. The future research should further optimize the test process, reduce the cost, and promote the update and perfection of international standards, so as to promote the sustainable development of automotive-level chip technology.

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