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Design of Periodic Signal Measurement and Analysis Device Based on Analog Preprocessing and FPGA Parallel Processing

Shaoyi Sun *, Yichun Li, Weimin She

School of Electronic and Optical Engineering, Nanjing University of Science and Technology, Nanjing, 210094, China
#These authors contributed equally

* **Corresponding author**: (Email: 15533188817@163.com)

Abstract: Combining analog preprocessing with FPGA parallel signal analysis, this paper implements a device for time domain and frequency domain measurement of periodic signals. The system consists of amplifying circuits, a 7 order Butterwort h low pass filter, a 14 bit ADC chip Zynq 7020 and a serial port screen, and adopts analog digital joint filtering to improve anti interference performance. Through front end signal conditioning and digital calibration, the peak to peak input range reaches 0 500 mV with measurement error controlled within 5 mV. A 121 order FIR filter equalizes the analog passband, achieving simulation residual error less than 0.02 dB within 0 500 kHz passband and about 53.9 dB digital attenuation at 1 MHz. In the time domain branch, true RMS value is calculated and 1 or 3 cycles of waveform can be displayed. In the frequency domain branch, 4096 point FFT with Hann window is utilized for spectrum analysis, and the practical frequency error is basically wit hin 10 Hz. Test results demonstrate that the proposed device features wide measurement range, high precision and strong anti interference capability, and can stably complete multi parameter measurement and analysis for periodic signals.

Keywords: Periodic Signal Measurement, True RMS, Hann Window, FFT, Analog Digital Joint Filtering.

1. Introduction

Periodic-signal time-frequency measurement is fundamental for electronic test, power-system monitoring and signal-analysis instruments, which demands both accurate time-domain parameter acquisition and reliable spectrum estimation under complex interference backgrounds [1-2]. With the rapid development of FPGA and high-speed ADC devices, embedded measurement instruments gain advantages in real-time processing, parallel computation and hardware integration, and gradually replace bulky traditional desktop test equipment [3-4]. Nevertheless, pure-digital acquisition schemes are vulnerable to high-frequency out-of-band interference; aliasing distortion and ADC saturation caused by pre-sampling interference will degrade final measurement accuracy, which cannot be fully eliminated merely by post-stage digital filtering [5-6]. Therefore, combining analog preconditioning and digital post-processing becomes a practical way to improve anti-interference performance for periodic-signal measurement instruments. Complex field test environments often contain unknown high-frequency spurious components, which impose stricter requirements on the front-end anti-interference capability of test instruments. Poor preprocessing design will further enlarge amplitude and frequency measurement deviations for weak small-amplitude signals.

Numerous existing studies have explored FPGA-based signal measurement and spectrum-analysis implementations [7-8]. Most reported instruments adopt all-digital architectures, focusing on optimizing FFT windowing strategy, frequency-interpolation algorithm or real-time RMS calculation logic [9-10]. However, less attention is paid to cooperative optimization of analog pre-filtering and digital equalization. Many designs omit pre-sampling analog suppression for out-of-band high-frequency interference, which brings potential risks of aliasing and amplifier clipping under actual noisy test scenarios. Moreover, few works quantitatively analyze filter-order selection, front-end gain margin and error-source decomposition for joint analog-digital measurement systems, leading to insufficient theoretical support for practical hardware parameter determination. Most existing verification experiments are carried out under ideal laboratory conditions without adding out-of-band jamming signals. This makes it difficult to objectively evaluate the actual robustness of the instrument in real-world working scenarios.

To address the above-mentioned gaps, this paper proposes a periodic-signal measurement-analysis device that integrates analog preprocessing and FPGA parallel signal analysis. A 7-order Butterworth low-pass filter is adopted for pre-sampling interference suppression, while a 121-order FIR filter compensates pass-band amplitude roll-off. On the FPGA platform, parallel time-domain and frequency-domain computation is realized to obtain peak-to-peak value, true RMS and spectral components. Experimental tests verify that the presented device achieves high measurement precision and strong anti-interference capability. This device supports flexible switching between one-cycle and three-cycle waveform display to satisfy diverse observation demands. It also completes all measurement tasks within the required 2-second system response time.

2. System Design and Theoretical Analysis

2.1. Scheme Selection and Overall System Scheme

Two alternative schemes are evaluated according to design requirements. The first scheme is an all-digital processing

solution based on high-speed ADC and FPGA. The input signal is buffered and amplitude-adjusted before feeding into high-speed ADC. FPGA completes digital filtering, time-domain parameter calculation, decimation, windowing, FFT and display control. However, pure digital processing can only process sampled data. For test scenarios where single-frequency interference with peak-to-peak value of 200 mV and frequency above 1 MHz exists at the input terminal, such interference may occupy the ADC dynamic range or even cause clipping of the pre-amplifier and ADC. Meanwhile, high-frequency interference may alias into the effective frequency band after sampling. Even if the FPGA digital filter provides high stop-band attenuation, it cannot completely eliminate nonlinear distortion and aliasing errors generated before sampling.

The second scheme combines analog preprocessing with FPGA digital analysis. In the analog domain, amplitude conditioning and high-frequency interference suppression are performed in advance. The input signal passes through the BNC interface to the wide-band pre-amplifier circuit with fixed gain. The amplified signal goes through a low-pass filter to suppress interference above 1 MHz while preserving effective frequency components. Afterwards, a 14-bit high-speed ADC ADS6148 performs sampling, and FPGA executes FIR equalization filtering. Finally, measurement results are transmitted to the touch screen via high-speed serial port for display.

Scheme-1 has powerful parallel-processing capability but lacks pre-sampling suppression for high-frequency interference. Scheme-2 cooperates analog preprocessing and FPGA digital analysis. It improves measurement resolution for small-amplitude signals, effectively reduces overload and aliasing caused by interference above 1 MHz, and satisfies requirements on frequency resolution and 2-second system response time. Therefore, Scheme-2 is adopted in this design.

The overall workflow adopts 4-times fixed gain to improve the utilization ratio of small-signal against ADC dynamic range. A 7-order Butterworth analog low-pass filter suppresses interference above 1 MHz before sampling. A 121-tap digital FIR compensates pass-band roll-off and further suppress residual high-frequency components. The high-performance ADS6148 ADC runs at 20 MSPS with 14-bit resolution. The time-domain branch keeps the original sampling rate, while the frequency-domain branch performs 10-times decimation down to 2 MSPS, yielding 488.28125 Hz frequency bin interval for 4096-point FFT. FPGA adopts parallel-pipeline architecture to simultaneously calculate peak-to-peak value, true RMS, fundamental frequency, spectrum and amplitude of each component. The whole device is powered by single external 5 V input; ±5 V required by AD603 is generated by on-board auxiliary power supply. This overall design balances small-signal measurement accuracy, high-frequency interference rejection, frequency resolution, waveform display quality and the 2-second response-time requirement. In addition, ADS6148 with high SNR and low aperture jitter is selected for 20 MSPS sampling. Combined with FIR filtering, Hann-window processing, spectrum-peak refinement and sampling-clock calibration, frequency-estimation stability is enhanced. The screen outputs floating-point data with two decimal places, achieving 10 Hz display resolution with typical measurement error within 10 Hz. Figure 1 illustrates the full-process design workflow.

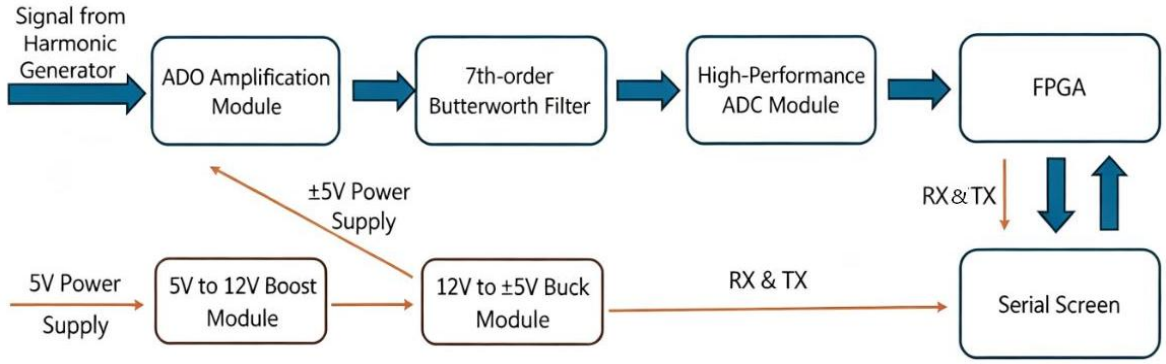

Figure 1. Overall design process

2.2. Front-end Fixed-Gain Analysis

The minimum peak-to-peak value of measured signal is 50 mV. Directly feeding small signals into ADC will make them occupy only a small fraction of full-scale input, so quantization noise, zero offset and external noise will exert remarkable influence on measurement results. Therefore, AD603 is used for fixed-gain amplification.

Considering that the maximum input voltage is 250 mV and the ADC input must be lower than 1.8 V, 4-times amplification provides sufficient safety margin. After 4-times front-end gain, the equivalent ADC LSB referred to device input is calculated. The theoretical quantization resolution is obviously better than the 5 mV error tolerance specified in requirements. In practical conditions, measurement errors mainly originate from amplifier gain deviation, ADC noise, analog filter amplitude-frequency characteristics and calibration error, rather than intrinsic ADC quantization interval.

The ADC calibration coefficient is about 291μV/code. After 4-times front-end gain, the single ADC code referred to the device input is:

$$K_{in}=\frac{291}{4}=72.75\mu V/code \quad (1)$$

The allowed 5 mV voltage error corresponds to:

$$N_{5mV}=\frac{5mV}{0.07275mV/code}\approx 68.7code \quad (2)$$

2.3. Order Calculation of Analog Low-Pass Filter

Butterworth filter and Chebyshev filter are two candidates. Under identical filter order, Chebyshev filter has steeper transition band for attenuating 1 MHz interference, but it produces pass-band ripples. Frequency-dependent ripples will convert into amplitude measurement error and increase calibration compensation burden. Butterworth filter features

maximally-flat pass-band response without ripples, and its amplitude-frequency response decreases monotonically with frequency. Its amplitude-frequency characteristic is:

Its amplitude-frequency characteristic is:

$$|H(jf)|^2=\frac{1}{1+\left(\frac{f}{f_c}\right)^{2n}} \quad (3)$$

For this design, the peak-to-peak value of 1 MHz interference can reach up to 200 mV, and the residual interference after filtering shall be no greater than 5 mV:

$$A_s=20\lg\frac{200}{5}=20\lg 40\approx 32.04\text{dB} \quad (4)$$

Set pass-band edge $f_p = 500\text{kHz}$ and stop-band frequency 1MHz. Calculation yields required filter order $n \geq 6.3$. Consequently, the 7-order Butterworth filter is selected, which provides about 38 dB attenuation at 1 MHz. Combined with subsequent FPGA digital filtering, it is unnecessary to exchange pass-band flatness for sharper cutoff. Chebyshev solution would demand extra frequency-dependent compensation inside FPGA and increase system complexity.

2.4. Digital Filtering and Fft Parameter Analysis

Only one external 5 V power supply is permitted, while amplifiers require ±5 V power rails. A 12 V-to-±5 V buck module is adopted. Nevertheless, two-stage power conversion leads to relatively low total efficiency. The single auxiliary power cannot simultaneously drive amplifier, FPGA and serial-screen within rated power rating. Additional pin-header parallel 5 V input is introduced for FPGA and serial-screen to guarantee stable operation of amplifier circuits.

Sampled data after analog filtering passes through a 121-tap FIR low-pass filter to further suppress residual high-frequency interference. The output of FIR filter can be expressed as:

$$y(n)=\sum_{k=0}^{120} h(k)x(n-k) \quad (5)$$

Where x is ADC sampling data and h is FIR filter coefficients. The filter adopts symmetric coefficient design. After FIR filtering, the FFT branch executes 10-times decimation to obtain 2 MSPS equivalent sampling rate, and then performs 4096-point FFT. The frequency interval is:

$$\Delta f=\frac{f_s'}{N}=\frac{2\times 10^6}{4096}=488.28\text{Hz} \quad (6)$$

The observation time of one FFT frame is 2 ms. The Hann window is applied to reduce sidelobe amplitude, so that small-amplitude harmonic components will not be covered by main-lobe spectral leakage. Since the Hann window reduces spectral amplitude, coherent-gain compensation is added for spectrum-amplitude conversion. If only the maximum FFT frequency bin is used for frequency estimation, the ideal maximum frequency quantization error is:

$$|e_f|_{max}\leq\frac{\Delta f}{2}\approx 244.14\text{Hz} \quad (7)$$

For AC true-RMS calculation, the root-mean-square value is directly computed by summing squares of sampling points, which does not rely on sinusoidal input. It can measure true-RMS values for sine, square-wave, triangular-wave and multi-harmonic composite signals:

$$U_{rms}=\sqrt{\frac{1}{N}\sum_{i=0}^{N-1}(U_i-\bar{U})^2} \quad (8)$$

3. Hardware and Software Implementation

3.1. Hardware Design

The hardware platform consists of BNC input interface, AD603 signal conditioning circuit, 7-order passive Butterworth low-pass filter, ADS6148 analog-to-digital conversion module, Zynq-7020 digital-processing unit, power-conversion circuits and serial-port liquid-crystal screen. Figure 2 shows the hardware circuit.

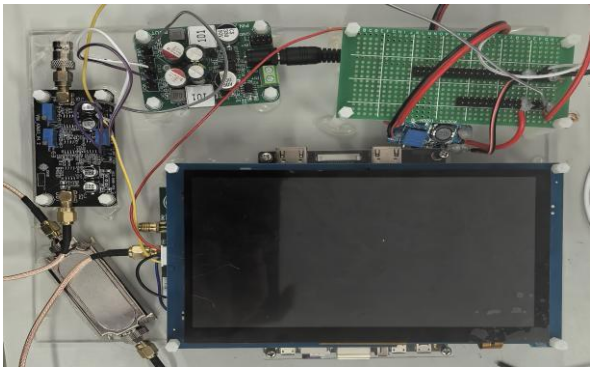

Figure 2. Hardware design

Periodic input signal enters via BNC connector and goes through analog filtering and AD603 gain conditioning to match signal amplitude with ADC input range. ADS6148 completes high-speed analog-to-digital conversion, and sampling data are sent to FPGA for parallel time-domain and frequency-domain processing. Finally, measured parameters and waveform data are transmitted to display via serial port, supporting visualization of one-cycle / three-cycle waveform, spectrum and related parameters. The schematic of the 7-order Butterworth filter is implemented with discrete inductors and capacitors. Figure 3 shows the circuit diagram of a seventh-order Butterworth filter.

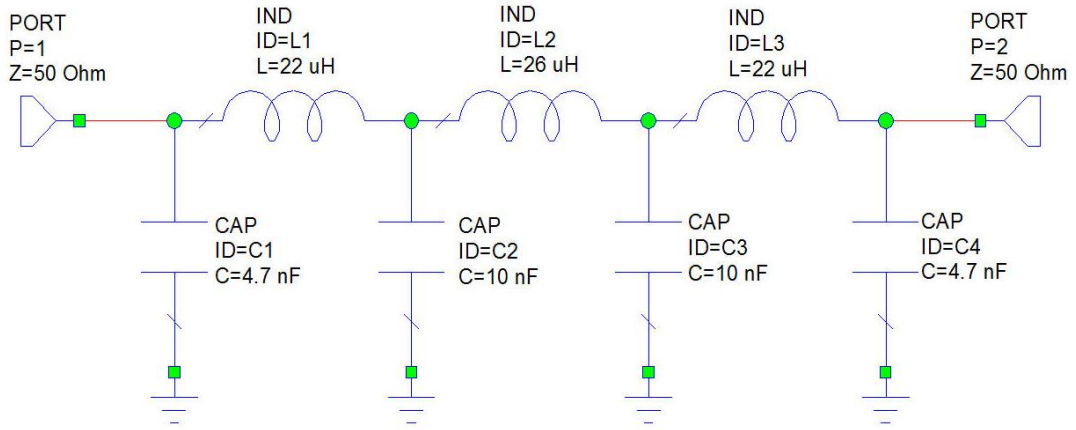

Figure 3. 7th-order Butterworth filter circuit diagram

3.2. Software Design

UART bidirectional communication between FPGA and serial-port screen works at baud-rate 921600 bit/s. FPGA converts peak-to-peak, true-RMS, frequency and waveform data into screen-recognizable instructions for parameter and waveform rendering. The serial-screen returns key-press commands such as page switch and 1-/3-cycle waveform selection. When communication fails, users trigger "re-connect" button; the screen resends connection request and FPGA restores data transmission and screen refresh. Full-frame data latch and sequential sending mechanism ensure synchronization between measured parameters and waveform graphics and improve communication reliability.

After receiving ADC samples, the system firstly performs digital FIR filtering. Data are then separated into parallel time-domain and frequency-domain processing paths. The time-domain branch calculates voltage parameters and generates waveform data. The frequency-domain branch conducts spectrum analysis. Processing results are transmitted to display, and waveform-cycle number and display pages can be switched according to key-press instructions. Figure 4 shows the overall software design architecture diagram.

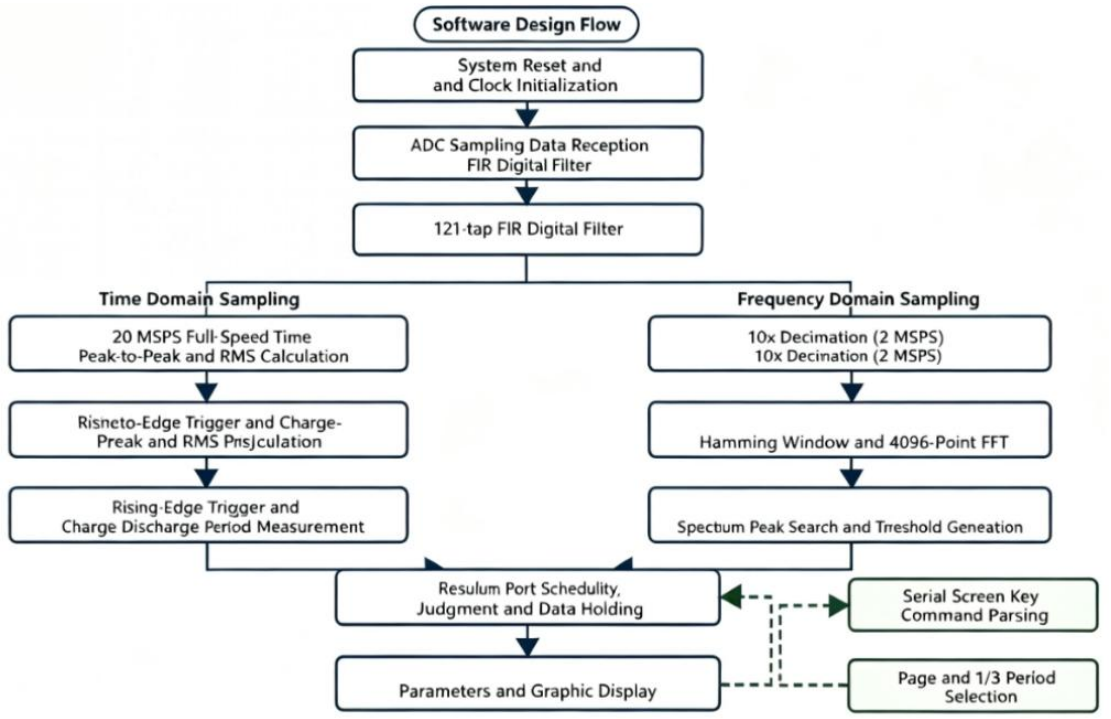

Figure 4. Overall software design diagram

4. System Test and Result Analysis

4.1. Test Method

A harmonic-capable signal generator serves as standard signal source with output impedance set to 50 Ω and connected to device input via BNC cable. The composite test signal contains 150 kHz fundamental wave (150 mV peak-to-peak), 300 kHz second-harmonic (250 mV peak-to-peak), and 450 kHz third-harmonic (50 mV peak-to-peak). After system output becomes stable, peak-to-peak value, true RMS and each frequency component displayed on screen are recorded and compared with generator preset values. Each group is measured repeatedly and stable readings are adopted for evaluation.

4.2. Test Results

Table 1 presents the measurement results obtained from the testing of composite periodic signals.

Table 1. Measurement results of composite periodic-signal test

Nominal fundamental frequency (kHz)	Nominal Vpp (mV)	Nominal Vrms (mV)	Measured Vpp (mV)	Measured Vrms (mV)	Measured fundamental frequency (kHz)	Vpp error (mV)	RMS error (mV)	Fundamental-frequency error (kHz)
150.00 (Fundamental)	150.00	53.04	150.45	53.67	150.01	0.45	0.63	0.01
300.00 (2nd harmonic)	250.00	88.40	249.46	87.94	300.00	0.54	0.46	0.00
450.00 (3rd harmonic)	50.00	17.68	50.32	18.35	450.00	0.32	0.67	0.00

5. Conclusions

This paper designs and implements a periodic-signal measurement and analysis device combining analog preprocessing and FPGA parallel processing. Through the cooperative work of 7-order Butterworth analog low-pass filtering and 121-order FIR digital equalization filtering, the system effectively suppresses out-of-band high-frequency interference before sampling. On the FPGA hardware platform, parallel time-domain and frequency-domain computing is realized to complete true-RMS, peak-to-peak value calculation and 4096-point FFT spectrum analysis. Experimental results based on multi-harmonic composite signals verify that the instrument achieves satisfactory measurement precision within 0-500 mV input range, and can switch between 1-cycle and 3-cycle waveform display while satisfying the 2-second system response requirement. Benefiting from the joint analog-digital anti-interference framework, the proposed device possesses favorable practicability for on-site electronic testing, power-signal monitoring and general-purpose laboratory measurement scenarios.

Nevertheless, the current system still has certain limitations. The present hardware is only validated under fixed sampling parameters, and automatic adaptive sampling rate adjustment for signals with drastically varying frequency is not supported; besides, the test cases are limited to multi-harmonic periodic signals without verification for complex non-stationary periodic signals. In future research, adaptive sampling rate control modules will be added to expand the applicable frequency range. Moreover, richer test signal types will be adopted for comprehensive validation, and more human-computer interaction functions will be integrated to further improve the versatility of this embedded measurement instrument.

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